Examiner D. Zarneke, is thanked for the thorough examination and search of the subject Patent Application. Claims 1-12 remain canceled per the restriction requirement.

The making FINAL of the Restriction requirement is noted.

Non-elected Claims 1-12 are hereby canceled. A divisional application will be filed to Claims 1-12 once the elected Claims are allowed.

All Claims are believed to be in condition for Allowance, and that is so requested.

Reconsideration of Claims 13-24 rejected under 35 U.S.C.

103(a) as being unpatentable over Yamaguchi (JP 405335313A) in

view of Yamai (JP 409045691) in view Forehand et al (U.S.

5,847,936) and in view Mars (U.S. 5,795,818) is requested based on the following remarks.

Applicant agrees with the Examiner that Yamaguchi describes a solder bump structure for an integrated circuit device.

However, Applicant does not agree that Yamaguchi teaches

Applicant's claimed invention, as recited particularly in Claims

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13 and 18. In particular, Applicant's claimed invention features a solder bump structure with a pillar 38 and 40 and a solder bump 42 where the pillar structure specifically comprises two metals 38 and 40 and where the top pillar metal 40 overhangs the vertical edges of the bottom pillar metal 38. All of these features are shown in Applicant's Figs. 3 and 4. Further, all of these features are recited in Claims 13 and 18. In particular, Claim 13 reads, in part:

13. (Previously Presented) A semiconductor device package, comprising:

a semiconductor device, said device having been provided with points of electrical contact in an active surface thereof, said points of electrical contact having been provided with fine pitch, high reliability solder bumps, said solder bumps extending from said active surface of said semiconductor device over a height of columns of pillar metal, said columns of pillar metal being in contact with said points of electrical contact provided in the 10 active surface of said semiconductor device wherein said pillar metal comprises two metal layers, and wherein top said metal layer overhangs vertical edges of bottom said metal layer;

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a Ball Grid Array substrate, said BGA substrate having been provided with points of electrical contact over a first and a second surface thereof, said points of BGA substrate being connected to interconnect lines provided over the second surface of said BGA substrate;

a solder mask provided over said second surface of said BGA substrate;

said device being positioned over the second surface of said BGA substrate, said fine pitch, high reliability solder bumps facing said second surface of said BGA substrate, providing contact between said fine pitch, high reliability solder bumps and said points of electrical contact provided over said second surface of said BGA substrate;

electrical contact having been established between

said fine pitch, high reliability solder bumps and said

points of electrical contact provided over said second

surface of said BGA substrate by a process of solder

reflow;

said semiconductor device being encapsulated in a

molding compound, said molding compound surrounding said

device on all sides including said active surface of said

device;

contact balls making electrical contact with said

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points of electrical contact provided over said first

40 surface of said BGA substrate; and

electrical contact having been established between said solder balls inserted into said solder mask provided over said first surface of said BGA substrate and said points of electrical contact provided over said first surface of said BGA substrate by a process of solder reflow.

Applicant notes two of the above features, notably the presence of a metal pillar comprising two metal layers and wherein the top metal layer overhangs the vertical edges of the bottom metal layer.

Applicant has carefully reviewed the cited art of Yamaguchi. Applicant does not agree that Yamaguchi shows the above-described features of a metal pillar comprising two metal layers and wherein the top metal layer overhangs the vertical edges of the bottom metal layer. Applicant notes Examiner's statement describing "columns of pillar metal (25 & 17), said columns of pillar metal being in contact with said points of electrical contact provided in the active surface of said semiconductor device wherein said pillar metal comprises two metal layers (25 & 17), and wherein top said metal layer

overhangs vertical edges of bottom said metal." However,
Applicant does not believe that Yamaguchi describes these
features such that it would be obvious to one skilled in the art
that layer 17 overhangs the vertical edges of layer 25. In
particular, Applicant notes that the illustrations of Yamaguchi
showing the completed device, notably [3], [6], and [7], do not
clearly show layer 17 overhanging the vertical edges of layer
25. Further, Yamaguchi does not verbally describe layer 17 as
overhanging the vertical edges of layer 25. Therefore, in the
absence of a clear definition of the relationship between layers
17 and 25, Applicant does not believe that Yamaguchi describes
Applicant's claimed invention such that one skilled in the art
at the time of the invention would be able to practice the
invention.

Applicant has further carefully reviewed the cited art of Yamai, Forehand et al, and Marrs and has found that none of these references teach or suggest this key feature of Applicant's claimed invention. Further, it appears to the Applicant that Lin et al, Yamai, Forehand et al, and Marrs, separately or in combination, fail to teach or suggest this key feature in such a way as to allow one skilled in the art at the time of the invention to have practiced the invention.

Therefore, Applicant believes that the claimed invention, as

recited in Claims 13 and 18, is patentable over the cited art. Applicant therefore respectfully requests that the rejection of Claims 13 and 18 under 35 USC 103(a) be removed in the light of the above analysis. Further, Claims 14-16 and 19-24 represent patentably distinct, further limitations on Claims 13 and 18 that should not be rejected under 35 USC 103(a) if the rejections of Claims 13 and 18 are removed.

Reconsideration of Claims 13-24 rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaguchi (JP 405335313A) in view of Yamai (JP 409045691) in view Forehand et al (U.S. 5,847,936) and in view Mars (U.S. 5,795,818) is requested based on the above remarks.

Reconsideration of Claim 17 rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al (US Patent 6,426,281) in view of Yamai (JP 409045691) in view Forehand et al (U.S. 5,847,936) and in view Marrs (U.S. 5,795,818) and further in combination with Pao et al (U.S. 5,931,371) is requested based on Amended Claim 13 and on the following remarks.

Applicant applies the same analysis given above regarding the rejection of Claims 13-24 and additionally finds that the cited art of Pao et al does not teach or suggest the key feature

of Applicant's claimed invention as described above. Further, it appears to the Applicant that Yamaguchi, Yamai, Forehand et al, Marrs, and Pao et al separately or in combination, fail to teach or suggest this key feature in such a way as to allow one skilled in the art at the time of the invention to have practiced the invention. Therefore, Applicant believes that the claimed invention, as recited in Amended Claims 13 and 18, is patentable over the cited art. Applicant therefore respectfully requests that the rejection of Claim 13 under 35 USC 103(a) be removed in the light of the above analysis. Further, Claim 17 represents a patentably distinct, further limitation on Claim 13 that should not be rejected under 35 USC 103(a) if the rejections of Claim 13 is removed.

Reconsideration of Claim 17 rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al (US Patent 6,426,281) in view of Yamai (JP 409045691) in view Forehand et al (U.S. 5,847,936) and in view Marrs (U.S. 5,795,818) and further in combination with Pao et al (U.S. 5,931,371) is requested based on Amended Claim 13 an on the above remarks.

Applicants have reviewed the prior art made of record and not relied upon and have discussed their impact on the present invention above.

Allowance of all Claims is requested.

It is requested that should the Examiner not find that the Claims are now Allowable that the Examiner call the undersigned at 989-894-4392 to overcome any problems preventing allowance.

Respectfully submitted,

Dougla R Acharbel

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